

1 WHAT IS CLAIMED IS:

1 1. A method for processing data in a processor with an instruction,
2 wherein the data is related to an array of elements, the method comprising steps of:
3 loading a first value from a first location;
4 loading a second value from a second location;
5 comparing the first and second values to each other;
6 optionally storing a predetermined value in a destination based upon the
7 comparing step.

1 2. The method for processing data in the processor with the
2 instruction, wherein the data is related to the array of elements as recited in claim 1,
3 wherein:
4 the first location and second location are source registers, and
5 the destination is a destination register.

1 3. The method for processing data in the processor with the
2 instruction, wherein the data is related to the array of elements as recited in claim 1,
3 wherein the first and second values are operands.

1 4. The method for processing data in the processor with the
2 instruction, wherein the data is related to the array of elements as recited in claim 1,
3 wherein the predetermined value is zero.

1 5. The method for processing data in the processor with the
2 instruction, wherein the data is related to the array of elements as recited in claim 1,
3 wherein the comparing step comprises determining if the array index is greater than or
4 equal to zero and less than a length of the array.

1 6. The method for processing data in the processor with the
2 instruction, wherein the data is related to the array of elements as recited in claim 1,
3 wherein the destination includes a base address for the array.

1 7. The method for processing data in the processor with the
2 instruction, wherein the data is related to the array of elements as recited in claim 1,
3 wherein the storing step further includes setting a flag.

1 8. The method for processing data in the processor with the
2 instruction, wherein the data is related to the array of elements as recited in claim 1,
3 wherein the first and second values are at least one of a signed integer and an unsigned
4 integer.

1 9. The method for processing data in the processor with the
2 instruction, wherein the data is related to the array of elements as recited in claim 1,
3 wherein the first location comprises a length of the array.

1 10. The method for processing data in the processor with the
2 instruction, wherein the data is related to the array of elements as recited in claim 1,
3 wherein the second location includes an index of the array.

1 11. The method for processing data in the processor with the
2 instruction, wherein the data is related to the array of elements as recited in claim 1,
3 wherein:

4 the first location includes a length of the array
5 the second location includes an index of the array.

1 12. An instruction processor that operates upon a first source register
2 having a first operand and a second source register having a second operand, comprising:
3 an operand compare function which compares the first and second
4 operands;
5 decision logic coupled to the operand compare function which determines
6 if the second operand is at least one of greater than zero and equal to zero; and
7 a flag setting function coupled to the decision logic.

1 13. The instruction processor that operates upon the first source
2 register having the first operand and the second source register having the second operand
3 of claim 12, wherein the flag setting function stores a zero in a destination register.

1 14. The instruction processor that operates upon the first source
2 register having the first operand and the second source register having the second operand
3 of claim 12, wherein the operand compare function loads the first and second operands
4 respectively from a first and second source registers.

1 15. The instruction processor that operates upon the first source
2 register having the first operand and the second source register having the second operand
3 of claim 12, wherein the flag setting function is coupled to a destination register.

1 16. A method for processing an array by a processor, the method
2 comprising the steps of:
3 determining if an array index is valid;
4 replacing a base address with a predetermined value based upon results
5 from the determining if an array index is valid step; and
6 determining if a base address of the array is valid.

1 17. The method for processing the array by the processor of claim 16,
2 further comprising the step of loading a first and second very long instruction words,
3 where each includes a plurality of sub-instructions.

1 18. The method for processing the array by the processor of claim 17,
2 wherein the first and second very long instruction words accomplish the determining
3 steps and a step of loading an array element at an index address.

1 19. The method for processing the array by the processor of claim 16,
2 wherein the predetermined value is an invalid base address.

1 20. The method for processing the array by the processor of claim 16,
2 further including the step of calculating an address offset.

1 21. The method for processing the array by the processor of claim 16,
2 further including the step of adding an address offset to the base address.

1 22. The method for processing the array by the processor of claim 16,
2 wherein the predetermined value is zero.

1 23. The method for processing the array by the processor of claim 16,
2 wherein the step of determining if array index is valid includes the steps of:
3 determining if the array index is with a range from zero to an array length
4 minus one; and
5 determining if the array index is less than the array length.